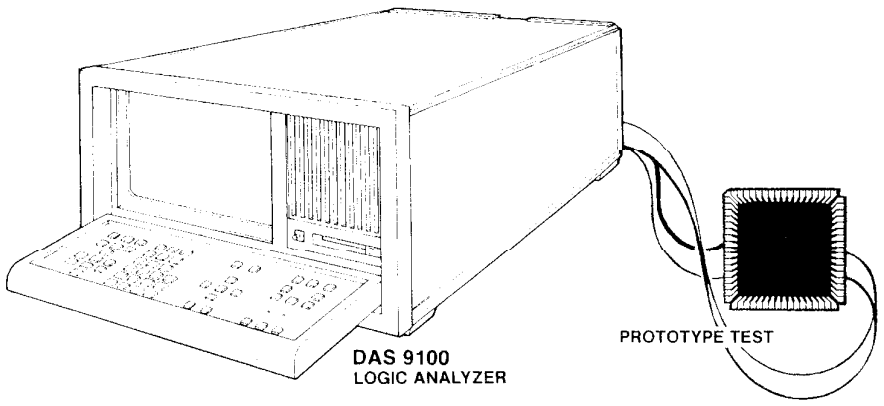
NEW

91DVV DesignLink® DAS VLSI VERIFICATION SOFTWARE PACKAGE

- Links DAS 9100 to VAX Host for Bench-Top VLSI Testing
- Uses Logic-Simulation Test Vectors for Prototype Test
- Vector Compression Increases Effective DAS Pattern Generator Depth
- Compares Predicted Outcomes to Actual Prototype Responses
- Rapid Setup Changes for Different Users and Prototypes
- C Source Code Operates in UNIX 4.1 bsd Environment
- Modular Software Is Easily Installed and Portable



The 91DVV DesignLink® DAS VLSI Verification Software is based on the UNIX software environment, and is designed to provide communications capabilities between a VAX host and the DAS 9100 Series digital analysis system. 91DVV is an easily set up and low-cost alternative to production test systems for prototype device verification.

91DVV enables hosted programming of pattern generation, data acquisition, and comparison between predicted and actual device responses. The 91DVV software converts test-vector tables into compressed DAS pattern generator programs, which it then downloads to the DAS for stimulation of the device. The protoype's resulting outputs are acquired by the DAS and uploaded to the host, where 91DVV compares the actual to predicted responses.

91DVV is an especially well-suited tool for creating an IC design-simulation and prototype-test system. 91DVV saves you time and promotes development continuity by using test vectors already developed for logic simulation. This also helps in verifying the simulation software's performance.

The 91DVV software package is straightforward to use. Hardware setup consists of connecting DAS pattern generator and data acquisition probes to a powered test fixture, which holds the prototype device. The 91DVV software automatically queries the DAS to determine the current DAS hardware configuration, and uses the information to set up the prototype test and comparison. A prompting dialogue helps you set up clocking, tri-state control, and vector-to-pin mapping.

The 91DVV software modules convert the test vectors into the DAS format and download them to the DAS pattern generators. The DAS exercises the prototype device and collects the responses, which 91DVV uploads to the host. 91DVV compares predicted responses to those actually acquired by the DAS, and outputs the results as a formatted listing. Test setups, routines, and results may be stored on the host, allowing rapid setup changes for multiple prototypes and users.

91DVV SOFTWARE MODULES

91DVV software is composed of several modules which act as UNIX shell commands. See Figure 1.

TLOGS2PAT

Converts a logic simulator's stimulus/response vector files into an easily processed intermediate format.

DASXFER

Converts the intermediate vector file into a form the DAS can use in its specific configuration.

DASPAC

Compresses the DASXFER output and compiles it into DAS binary packets. DASPAC supports the entire DAS pattern generator instruction set, including REPEAT, COUNT, HOLD, GOTO, CALL, RETURN, and HALT. It also supports labels used for GOTO and CALL references.

PUTPAC

Downloads DAS binary packets from the UNIX environment to the DAS.

GETACQ

Uploads contents of the DAS acquisition memory (up to 104 channels) to the UNIX environment.

CMPACQ

Compares predicted device responses to the outputs acquired by the DAS.

GETPAC

Uploads DAS binary packets to the UNIX environment.

ADVANCED UTILITIES

Two advanced DAS utilities; SENDD and BDUMP are included with 91DVV to aid installation and debugging.

DAS LIBRARY ROUTINES

The DAS library is a set of low-level routines that provide straightforward access to the DAS. The routines support binary block expansion and compression, DAS system control, and low-level I/O functions.

TRI-STATE SUPPORT

The 91DVV software supports use of P6457 tri-state pattern generator probes, and also supports two methods for controlling customer-supplied tri-state buffers.

OPERATING ENVIRONMENT

91DVV runs on the VAX 782, 780, 750, 730, and 725 mainframes. It requires the UNIX 4.1 bsd (Berkeley) operating system. As source code is provided, the advanced user can adapt 91DVV to other UNIX versions. 91DVV is customer installed. UNIX makefiles are provided to ease system installation, compilation, and documentation.

COMPATIBILITY

91DVV can be modified to read any logic simulator's test vectors when output as a standard UNIX text file. 91DVV is supplied with an example simulator-to-91DVV front-end module, and with a description of the intermediate file format used. 91DVV is compatible with all DAS mainframe configurations. All DAS keyboard and menu functions remain operable when used with 91DVV. DAS modules supported are: 91A32 and 91A08 data acquisition modules; 91P16 and 91P32 pattern generator modules. DAS probes supported are: P6452 and P6454 data acquisition probes; P6455, P6456, and P6457 pattern generator probes. 91DVV supports DAS Option 06 I/O communications options through the RS-232 link.

ORDERING INFORMATION

91DVV1F DAS VLSI Verification Software Package (Release 1), TU-58 cassette tape **$1,000**

91DVV1G DAS VLSI Verification Software Package (Release 1), Nine track ½ inch tape, 800 BPI density **$1,000**

91DVV1H DAS VLSI Verification Software Package (Release 1), Nine track ½ inch tape, 1600 BPI density **$1,000**

Ask about 91DVV versions for other computers and operating systems.

GPIB DAS 9100 SERIES

Digital Analysis System

The DAS 9100 Series Option 06 complies with IEEE Standard 488-1978, and with Tektronix *Standard Codes and Formats*.

Color Display Enhances Ease-of-Use and Increases Productivity

Nine Standard Application Configurations Available or Custom Design Your Own System

Acquisition Speeds to 660 MHz (1.5 ns)

Data Widths to 104 Channels

Pattern Generation Up to 80 Channels at 25 MHz

Color, Monochrome and ATE Mainframes

Modular Architecture for the Future

DesignLink® Software Links DAS 9100 to a Host for Bench Top VLSI Functional Testing

Disassembly Support for Over 30 Microprocessors and Buses

Memory Depths from 512 to 4096 Bits Per Channel

Patented EDM Disassembles Proprietary Processors and Buses

Select Triggering to 16 Levels

Patented Time Correlation of High- And Low-Speed Data

Separate Glitch Memory

State-Table and Timing Diagrams Displayed for all Channels

Pattern Generation to Simulate Hardware or Software

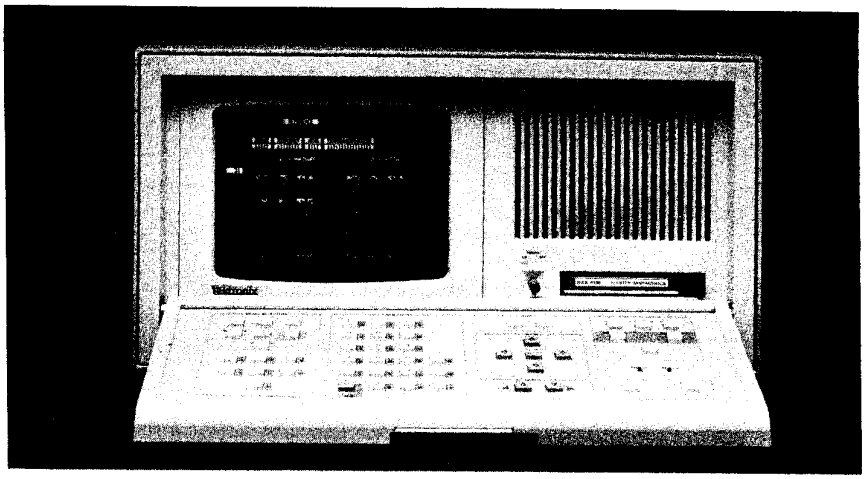
Delta Time and Auto-Run Mode

Supports GPIB, RS-232, Hard-Copy Units and Serial Line Printers

Tape Drive Stores Patterns and Instrument Set-Ups for Future Use

The Industry Standard

The DAS 9100 Series Digital Analysis System has set the industry standard for virtually all aspects of logic analysis. Its modular mainframe accepts a wide assortment of both data acquisition and pattern generation modules to fit your application needs. You get performance combinations unavailable in any other logic analyzer, including data widths to 104 channels and acquisition speeds up to 660 MHz. Another DAS 9100 innovation is the inclusion of pattern generation modules, up to 80 channels, which can be used in concert with data acquisition modules to perform sophisticated test procedures, such as VLSI Functional Test.



Also, the DAS is unmatched in its ability to adapt to almost any engineering work environment. It has the capacity to interface with mainframes, GPIB controllers, development systems and other DASs. For stand-alone situations, there's a built-in tape storage unit and the DAS outputs to both hard copy units and serial line printers.

The Leader in Ease-of-Use

The DAS 9100 has an unmatched feature set that makes it the undisputed leader in ease-of-use. The Color DAS 9129 is currently the only logic analyzer available on the market with a color-coded CRT. Each of the instrument's setup menus and data displays are organized into color groups which promote faster interaction, better understanding, reduce chance of error and minimize fatigue.

The color coding scheme is the product of intensive research by Tektronix into the use of color to enhance user productivity during interaction with a CRT display. The CRT supports three colors, red, yellow and green, plus the black background. These color phosphors fall within a common focal depth, which means the eye does not have to refocus when scanning from one color to another.

See this color product in the reference section beginning on page 17.

Green (a "quiet" color), is used to display supporting information in an unobtrusive manner. Yellow (a more agressive color), is applied to information of immediate interest, such as acquired data. Red, which attracts immediate attention, is reserved for exceptional situations, such as marking the trigger point in a data stream or listing illegal instructions during a disassembly.

Both the Color DAS and its monochrome counterpart have a menu-driven operating system which vastly simplifies all user interactions. Each particular function, such as trigger setup or pattern generation programming, has its own menu which is largely self-explanatory. The user simply moves the cursor to the appropriate video fields and supplies the required information. There is no need for lengthy manual references to master the instrument's operation. When a menu entry falls outside acceptable bounds, a message appears which explains the specific nature of the error, thus allowing simple recovery without the need for a separate help function.

The operating system also includes features which promote fast accurate analysis of acquired data. A reference memory compare color-codes all differences between acquisition and reference memories. The Delta Time feature allows precise measurements of the time interval located between movable cursors.

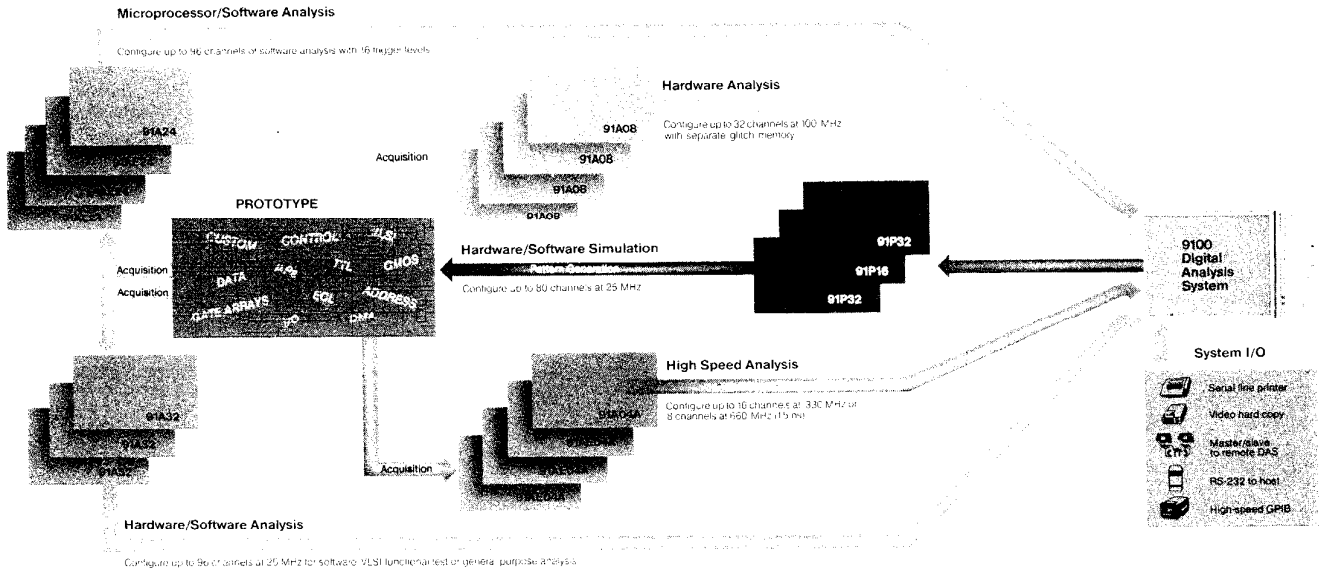
A major benefit in most engineering situations is the ability to retain instrument setups and reference data for future use. The DAS 9100 has a built-in DC 100 cartridge tape drive, which retains complete instrument setups as well as reference memory data and mnemonic definition tables used to disassemble acquired data. All tape drive I/O operations are accomplished through a simple, menu-driven filing system.

8-Bit and 16-Bit Microprocessor Design Support at its Best

In response to the overwhelming need for good microprocessor design support in logic analysis, the DAS 9100 Series offers a greater depth and range of microprocessor-based support than any other analyzer.

The key to this support is the DAS 9100's new Patented Extended Define Mnemonics, which allows the unit's built-in DC 100 tape drive to act as a storage medium for mnemonic tables for 8-bit, 16-bit and even custom processors.

EDM (Extended Define Mnemonics) is a powerful, table-driven program which is part of the DAS firmware. EDM performs disassembly of data acquired synchronously off a microcomputer system bus. EDM uses a series of nested tables to complete the disassembly. All address, data and control information is received by a master table and passed down through a hierarchy of tables which converts it into disassembled mnemonics. For custom processors, you can create your own set of tables. For commercial processors, Tek has a wide array of both 8-bit and 16-bit EDM tapes available, which will automatically complete the disassembly for you.



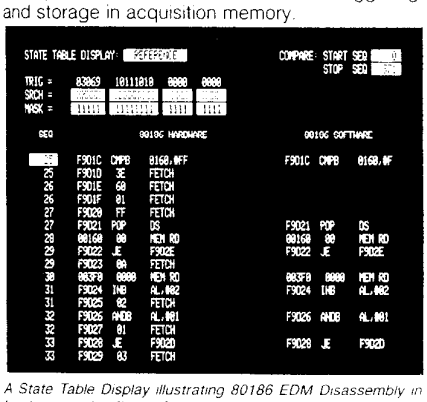
Select from one of the following support packages or use EDM to create a disassembly program for your own custom processor:

8080	6801	68010	1805
8031	6802	Z80	NSC800
8039	6803	Z8001	F9450
8085	6805	Z8002	1750A
8086	6808	Z8003	UNIBUS
8088	6809	Z8004	Q-Bus
80186	68121	6502	GPIB
80188	68000	65C02	ASCII
6800	68008	1802	EBCDIC

NOTE: For Ordering Information consult the microprocessor support section on pages 122 and 123.

Each 8-bit EDM disassembly tape includes a full set of disassembly tables and also a file containing all the setup parameters needed to have the 91A24 data acquisition modules acquire software transactions as executed on the system bus. For even further convenience, there is a Probe Interface Adaptor which allows all probe hookups to the processor to be completed in a single connection.

At the 16-bit level, EDM tapes are used in conjunction with the new PM 200 Series to complete the disassembly. Each PM 200 module probes the 16-bit processor under test and uses discrete logic to interpret data flow for disassembly, including operations such as clock synthesis and monitoring the fetch queue. The acquired data is then passed on to the DAS itself for triggering and storage in acquisition memory.



A State Table Display illustrating 80186 EDM Disassembly in hardware and software format.

Only the DAS 9100 allows you to select the disassembly format you need: Software, hardware or absolute.

At both the 8-bit and 16-bit level, EDM has a powerful and flexible feature set which makes the DAS 9100 the leader in software analysis support. EDM gives you three distinct types of disassembly: Software disassembly, which presents software flow in a similar format to an assembly listing; hardware disassembly, which shows mnemonics along with all processor cycles; and absolute disassembly, which identifies each bus cycle by type and gives the hexidecimal values associated with each cycle. EDM also allows user selectable color coding of displayed data and the addition of comments and labels. You can even use disassembly mnemonics when defining triggers with the 91A24 trigger menu.

SELECT YOUR CONFIGURATION

The DAS 9100 has six different data acquisition modules. Each has its own data width and maximum speed: 24 channels at 10 MHz for software analysis (96 channels maximum); 32 channels at 25 MHz (96 channels maximum); 8 channels at 100 MHz with glitch memory (32 channels maximum); 4 channels at 330 MHz (16 channels maximum) or two channels at 660 MHz (8 channels maximum). Modules can be combined to give you the logic analyzer you need.

Need high speed performance? One module can track your system clock (synchronously) at speeds to 330 MHz or provide asynchronous sampling to 660 MHz. The 8-channel module provides both synchronous and asynchronous sampling at 100 MHz. And the 32-channel or 24-channel module can be used to arm the trigger on those modules with higher acquisition rates.

To back it all up, there's powerful triggering, clock and trigger qualification, programmable reference memory and multiple clocks. There is glitch triggering, with a separate glitch memory for unambiguous glitch detection and our unique "arms mode" that allows precise timing correlation between synchronous and asynchronous data.

Arms mode allows the DAS 9100 to capture synchronous and asynchronous data simultaneously. The data is displayed in the correct time relationship for easy analysis in either Timing or State Display mode. To obtain the data width and speed your application requires, simply select the appropriate combination of modules and add on later as your needs change.

To enhance the tool set, the define mnemonics menus allow the user to build disassembly tables to support proprietary and other non-supported chips. Up to 64 tables with 256 entries per table can be nested to provide the capability to support complex 16-bit processors, with room left over!

Pattern generation makes it possible to start debugging hardware before your software, or all of your hardware, is available.

Pattern generation capability is built around a 16-channel, 25 MHz controller module. Through additional expansion modules, you can increase the total to 48 or 80 channels while maintaining full system speed. The pattern generator allows interaction with the prototype through clock outputs, data strobes, an external clock, and external control inputs, including an interrupt line. And, the pattern generated can even be changed, based on the data acquired by the logic analyzer, through the external control lines.

The DAS 9100 also offers you powerful I/O options, including a built-in magnetic tape cartridge drive (Option 01) to store instrument setups, pattern sequences, mnemonics and reference memory. The RS-232 and GPIB interface (Option 06) offers complete remote programmability and supports hard copy units, video displays and serial line printing. It enhances high-speed GPIB for ATE applications up to 200 kbytes per second transfer rate. Option 06 also provides an RS-232 line printer port for the DAS to allow for easy documentation of menu displays, EDM tables, state tables and timing diagrams.

Options 03 and 04 allow you to add one or two additional modular power supplies (each supply powers two slots). The standard DAS mainframe comes with a power supply for two slots. You only pay for the capability you need.

See page 114 for DAS 9100 module and option selection guide.

DAS 9100

SOFTWARE ANALYSIS MICROPROCESSOR & BUS SUPPORT	SOFTWARE & HARDWARE ANALYSIS GENERAL PURPOSE 25 MHz SUPPORT	HARDWARE ANALYSIS GENERAL PURPOSE 100 MHz SUPPORT
91A24 and 91AE24	91A32	91A08
DATA ACQUISITION MODULES	DATA ACQUISITION MODULE	DATA ACQUISITION MODULE
16 Level Sequential Trigger Tracing	32 Channel Data Width	Synchronous or Asynchronous Sampling to 100 MHz
Data Storage Qualification with up to 4 Word Recognizers	Synchronous or Asynchronous Sampling to 25 MHz	8 Channel Data Width Expandable to 32 Channels
32 Bit Counter/Timer with 100 ns Resolution	3 Word Recognizers with Occurrence Counter	5 ns Glitch Trigger and Storage
24 Data Channels with 1 K Memory Depth	2 Clock Qualifiers and Expandable Clocking	Separate Glitch Storage Memory
3 External Clocks and 3 Qualifiers with Independently Programmable Expressions	Arms 91A08 and 91A04A	Trigger Arming From 91A24 or 91A32
Single Probe Demultiplexing		
Synchronous or Asynchronous Acquisition, Down to 100 ns Data Cycles		
Supports Over 30 Microprocessors and Buses with 91TMXX Support Series (Page 123)		

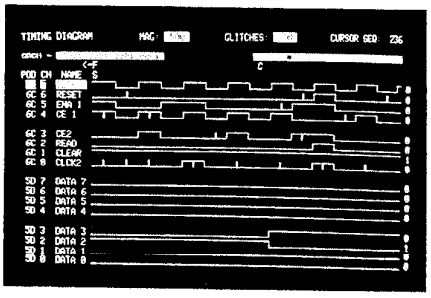
For software analysis, the 91A24 data acquisition module provides advanced triggering and clocking. It employs five independent word recognizers which include a 16 level stack that lets you build the complex triggers and data qualifiers necessary to debug involved software routines.

Maximum Modules Per DAS — One 91A24 maximum per DAS mainframe, three 91AE24 expansion units maximum per DAS mainframe (requires 91A24 to operate).
Maximum Number of Inputs — 24 data channels expandable to 96 channels with one 91A24 and three 91AE24 modules.
Maximum Sampling Rate — 10 MHz internal or external clock, 100 ns cycle time.
Memory Depth — 1023 bits per channel.
Reference Memory — 1 k by 48 channels formattable to 512 by 96 channels, compare with acquisition, trigger on compare equal or not equal, column masking and programmable compare window.
Clock Qualifiers — Three available on 91A24 only. Selectable polarity for each of three POD clock expressions.
Clock — Selectable from one internal or three external sources.
Internal: 100 ns to 5 ms ±01% ±01 ns.
External: Three clock inputs, 20 MHz maximum, selectable rising or falling edge for each of three independent Boolean clock expressions, one expression per POD memory, [(CLK1 • Q1) + (CLK2 • Q2) + (CLK3] • Q3. Demultiplex mode with 50 ns DEMUX interval minimum and 100 ns cycle minimum.
Triggering — Five independent word recognizers with selectable operating modes:
WR1 — Begin store or store only data qualifier.
WR2 — Begin store or store only data qualifier or parallel trigger event.
WR3 — 16 level sequential trigger stack with occurrence counter and sync output or counter/timer control option at each stack level.
WR4 — END store data qualifier, RESET stack operation, or OFF.
WR5 — END store data qualifier or OFF.
External trigger enable input and trigger sync output.
Trigger Positioning — BEGIN, CENTER, END, or DELAY 1 to 32,767 clocks
Trigger Arming — Arms 91A08 or 91A04A.
Event Counter — Counts from 1 to 4,096 events programmed on individual stack levels.
Probes — P6460 or P6462, three per module; mixing probes is not recommended.
Data Set Up Time — 25 ns minimum using P6460, 29 ns minimum using P6462.
Data Hold Time — 0 ns maximum using P6460, 3 ns maximum using P6462.
Qualifier Set Up Time — 25 ns minimum using P6460, 29 ns minimum using P6462.
Qualifier Hold Time — 0 ns maximum using P6460, 3 ns maximum using P6462.
Counter/Timer — 32 bit, 100 ns resolution START or STOP from stack levels.

In many instances, the engineer's goal is to monitor overall logic activity on the system bus. Here the 91A32 data acquisition module becomes an ideal choice. It combines a 32-channel data width with sample rates up to 25 MHz. To define and capture various types of bus transactions, each 91A32 module has three levels of triggering and two clock qualifiers. Up to three 91A32 modules may be used in a single DAS mainframe, for a total of 96 parallel channels.

Maximum Modules Per DAS — Three 91A32 modules max per DAS mainframe.
Maximum Number of Inputs — 32 data channels expandable to 96 channels with three modules.
Maximum Sampling Rate — 25 MHz internal or external clock, 40 ns cycle time.
Memory Depth — 512 bits per channel.
Reference Memory — 512 bits/channel, compare with acquisition, trigger on compare equal or not equal, column masking and programmable compare window.
Clock Qualifiers — Two per module six maximum, selectable polarity.
Clock — Selectable from one internal or up to three external sources.
Internal: 40 ns to 5 ms ±01% ±01 ns.
External: Selectable rising or falling edge, demultiplex split clock mode available with two or three 91A32 modules.
Triggering — Three word recognizers, two provide sequential or independent triggering with occurrence counter, one provides independent reset function. External trigger enable input and word recognizer output.
Trigger Positioning — BEGIN, CENTER, END or DELAY 1 to 32,767 clocks.
Trigger Arming — Arms 91A08 or 91A04A.
Event Counter — Counts from 1 to 32,767 word recognizer events.
Probes — P6452 or P6462, four per module; mixing probes is not recommended.
Data Setup Time — 29 ns minimum using P6452, 25 ns minimum using P6462.
Data Hold Time — 0 ns maximum using P6452, 7 ns maximum using P6462.
Qualifier Setup Time — 29 ns minimum using P6452, 25 ns minimum using P6462.
Qualifier Hold Time — 0 ns maximum using P6452, 7 ns maximum using P6462.

Many applications call for asynchronous sampling to observe the status of control lines during bus transactions. For this purpose, the 91A08 data acquisition module serves as an ideal tool. Each 91A08 gives you 8 data channels at sample speeds up to 100 MHz and independent glitch triggering. A single DAS mainframe will accept four of these modules for a total of 32 channels at 100 MHz.



91A08 Timing diagram with glitches

Maximum Modules Per DAS — Four 91A08 modules maximum per DAS mainframe.
Maximum Number of Inputs — Eight data channels expandable to 32 channels with four modules.
Maximum Sampling Rate — 100 MHz internal or external clock, 10 ns cycle time.
Memory Depth — 512 bits per channel with separate 512 bits per channel for glitch storage.
Reference Memory — 512 bits per channel, compare with acquisition, trigger on compare equal or not equal, column masking and programmable compare window.
Clock Qualifier — One per module, four maximum, selectable polarity.
Clock — Selectable from two internal or two external sources.
Internal: 10 ns to 50 ms ±01% ±01 ns.
External: Selectable rising or falling edge.
Triggering — Single level word recognizer and glitch recognizer. External trigger enable using arms mode.
Trigger Positioning — BEGIN, CENTER, END or DELAY 1 to 32,767 clocks.
Trigger Arming — Armed by 91A24 or 91A32.
Probes — P6452, one per module.
Data Setup Time — ≤9 ns using one 91A08, ≤10 ns using multiple 91A08 modules.
Data Hold Time — 0 ns maximum.
Qualifier Setup Time — ≤9 ns using one 91A08, ≤10 ns using multiple 91A08 modules.
Qualifier Hold Time — 0 ns maximum.
Glitch Storage — 5 ns minimum glitch width.

DAS 9100

HARDWARE ANALYSIS HIGH-SPEED 330 MHz or 660 MHz SUPPORT	PATTERN GENERATION GENERAL PURPOSE STIMULUS SUPPORT	GPIB, RS-232, TAPE DRIVE, LINE PRINTER & HARD COPY SUPPORT
91A04A and 91AE04A	91P16 and 91P32	OPTIONS 01 & 06
DATA ACQUISITION MODULE	PATTERN GENERATOR MODULES	COMMUNICATION INTERFACE OPTIONS
1.5 ns Sample Interval in Two Channel Mode For 660 MHz Asynchronous Acquisition	Stimulus Data and Clock Rates to 25 MHz	High Speed GPIB (200 kbytes/second)
Synchronous Acquisition to 330 MHz	Data Widths of 16, 48 or 80 Output Channels	RS-232 Host Interface
Asynchronous Acquisition to 330 MHz on All 4 Channels	Up to 10 Independently Programmable Strobes	RS-232 Line Printer Port
4 Data Channels With 2048 Bits Per Channel Memory Depth	Programmable Tri-State Output Control	RS-232 Master/Slave Operation
4096 Bits Per Channel in Two Channel, 1.5 ns Mode	External Pause, Tri-State, and Interrupt Control Inputs	Video Out/Hard Copy Support DC 100 Tape Drive Local Storage
Trigger Arming From 91A24 or 91A32	Vector Count, Hold, Repeat, and Looping Operations	
Auto-Deskewing Minimizes Channel-To-Channel Skew and Ensures Optimum Setup and Hold Times	Vector Sub Routine, Nested up to 16 Levels	

For high-speed hardware analysis, select the 91A04A data acquisition module which delivers sample speeds up to 660 MHz, the fastest in the industry. This extremely fast asynchronous sample rate gives you a timing resolution of 1.5 ns, fast enough to actually capture and display glitches in their true timing relationship to other signals. Now you can truly analyze where those errant pulses originated.

Maximum Modules Per DAS — One 91A04A maximum per DAS mainframe, three 91AE04A expansion units maximum per DAS mainframe (requires 91A04A to operate).

Maximum Number of Inputs — Four data channels expandable to 16 channels with one 91A04A and three 91AE04A modules.

Maximum Sampling Rate — 660 MHz internal two channels only (1.5 ns sample interval), 330 MHz internal clock four channels (3 ns cycle time), 300 MHz external clock four channels (3.3 ns cycle time).

Memory Depth — 2048 bits per channel; 4096 bits per channel in two channel 1.5 ns mode only.

Reference Memory — 512 bits per channel, compare with acquisition, trigger on compare equal or not equal, column masking and programmable compare window.

Clock Qualifiers — None.

Clock — Selectable from one internal or one external source.

Internal: 1.5 ns to 5 ms.

External: Selectable rising or falling edge.

Triggering — Single level word recognizer. (In 1.5 ns mode only trigger word must be valid for one sample period ± 2.5 ns). External trigger enable using arms mode.

Trigger Positioning — BEGIN, CENTER, END or DELAY by 1 to 32,767 clocks.

Trigger Arming — Armed by 91A24 or 91A32.

Event Counter — None.

Probe — P6453, one per module included.

Data Setup Time — 3.0 ns worst case adjustable in 400 ps increments.

Data Hold Time — 0.3 ns worst case adjustable in 400 ps increments.

Qualifier Setup Time — NA.

Qualifier Hold Time — NA.

Channel to Channel Skew — 0.50 ns on rising edges typical, 0.90 ns on falling edges typical.

Minimum Detectable Pulse Width — 3.5 ns worst case.

Pattern generation makes it possible to start debugging hardware before your software, or all of your hardware, is available. The basic 91P16 Pattern Generator module gives you 16 channels of circuit stimulation at up to 25 MHz, and expansion modules can raise the total to 80 channels.

Maximum Modules Per DAS — One 91P16 maximum per DAS mainframe, two 91P32 maximum per DAS mainframe (requires 91P16 to operate).

Maximum Number of Outputs — 16 data channels and two strobes expandable to 80 data channels and 10 strobes with one 91P16 and two 91P32 modules.

Maximum Stimulus Rate — 25 MHz internal or external clock, 40 ns cycle time.

Pattern Memory Depth — 254 words or instructions, able to output over 65,000 unique patterns single pass or continuous.

External Control Lines — Three available from trigger time base probe.

Pause — Holds pattern output temporarily while asserted, selectable polarity.

Inhibit — Tri-States all outputs while asserted, selectable polarity.

Interrupt — Forces jump to subroutine after asserted. Selectable rising or falling edge.

Clock — Selectable from one internal or one external source and single step operation.

Internal: 40 ns to 5 ms ±.01% ±.01 ns.

External: Selectable rising or falling edge.

Instruction Set — Seven commands available to program sequence and pattern vector output.

COUNT (N) — Increment A pattern N times, one per clock.

HOLD (N) — Hold pattern output and inhibit clock for N cycles.

REPEAT (N) — Hold pattern output while generating N clock cycles.

GOTO (LABEL) — Output patterns starting at LABEL.

CALL (LABEL) — Call pattern subroutine at LABEL.

RETURN — Return from subroutine call.

HALT — Output pattern and inhibit clock.

Number of (N) Variables — Six maximum.

Number of Labels — 32 maximum.

Number of Nested Subroutines — 16 maximum.

Number of Strobes — Two strobe outputs on 91P16, four strobe outputs on 91P32.

Strobe Pulse Polarity — Selectable positive or negative.

Strobe Delay Time — Selectable from 70 ns to 40.910 μs in 40 ns steps.

Strobe Pulse Width — Selectable from 40 ns to 40.880 μs in 40 ns steps.

Clock Output — One clock line per probe, rising edge signifies beginning of cycle.

Probes — P6455 for TTL/MOS, P6456 for ECL, or P6457 for TTL/MOS with individual bit Tri-State. Two per 91P16 module, four per 91P32 module.

Output Data Skew — ≤10 ns.

Output Clock Skew — ±5 ns between different probes.

Pause Pulse Width — 19 ns minimum.

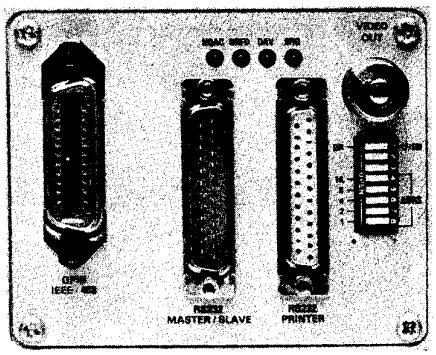
Pause Hold Time — 14 ns after output clock transition.

Inhibit Delay Time — 70 ns maximum.

Interrupt Setup Time — 7 ns minimum relative to external clock input, 72 ns minimum relative to output clock.

Interrupt Latency — 4 sequence execution delay.

The DAS Option 06 external communications package provides the most complete array of I/O capabilities to handle both computer and peripheral interfaces. It includes high speed GPIB, RS-232 master/slave, RS-232 printer port and hard copy interfaces. In the GPIB mode, host controller supplies all DAS menu setups and receives test results, with the DAS serving either as talker or listener. In the master/slave mode, one DAS acts as the master controller for a second DAS, which may be in a remote location and linked to the master DAS via modem. For stand-alone DAS installations, the RS-232 printer port and hard copy (video) output provide excellent documentation support for making copies of DAS menus and state or timing diagrams.



Rear Communications Interface panel Option 06

DAS 91DVV VLSI Verification Software uses the host communications capability of Option 06 to transfer test vector patterns to the DAS and to upload actual VLSI functional test data for host analysis.

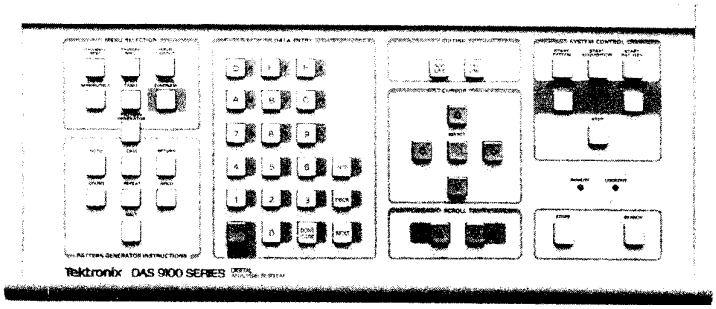
DC 100 Tape Drive Option 01

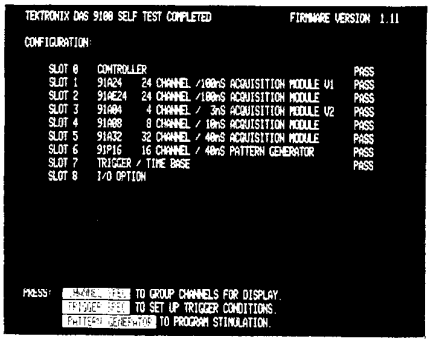
For workstation-type applications, the Option 01 built-in DC 100 tape drive provides convenient, menu-operated local storage and retrieval. It accepts tape cartridges (each holding up to 32 separate files) to store reference data, pattern generation programs, Extended Define Mnemonics tables or data acquisition setups.

DAS 9100 SERIES

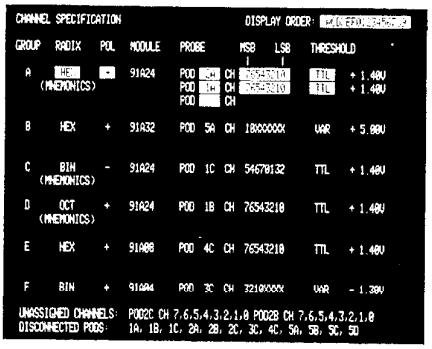
The Leader in Flexibility and Ease of Use Through Superior Human Engineering

Besides color, the DAS 9100 includes many other important human engineering features. Its menu-driven, user interface is easy to learn and self-documenting, so there is no need to constantly refer to manuals. To complement the menu-driven displays, there is a color-coded keyboard organized specifically to enhance user programming. All keys are arranged into logical groups that correspond to the display elements they service.

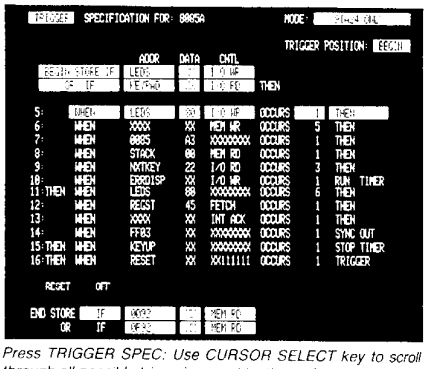




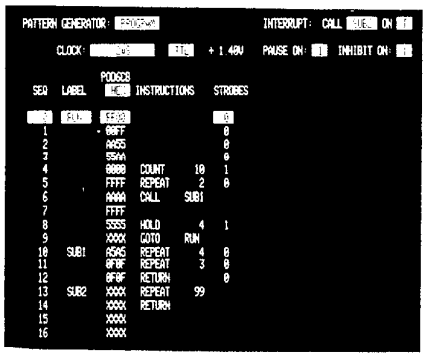
Pull POWER ON: A configuration menu appears describing all card modules in the DAS by slot number location. A sophisticated self-test verification is performed on each module with pass/fail indication. Bottom of screen indicates next step.



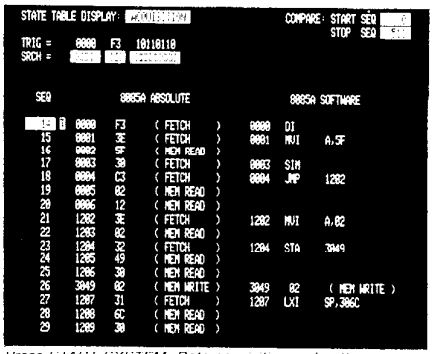
Press CHANNEL SPEC: Through the use of CURSOR and DATA ENTRY keys all data acquisition channels are assigned to groups, a group radix is selected (hex, binary or octal), and individual probe pod thresholds and channel order are user assigned.



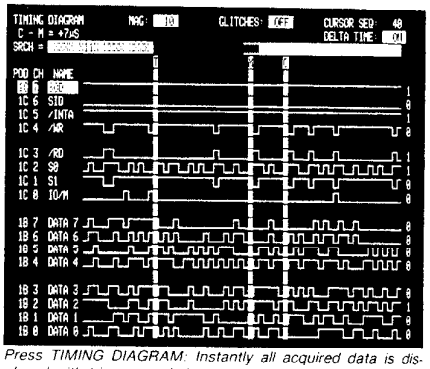
Press TRIGGER SPEC: Use CURSOR SELECT key to scroll through all possible triggering combinations of data acquisition modules, including "ARMS MODE". The 91A24's five word recognizers with 16-level stack are shown. Address and control fields symbolically display labels and control functions.



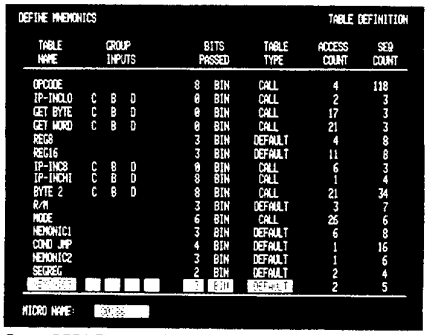
Press PATTERN GENERATOR: This menu allows you to construct a pattern generation program 254 lines deep using English-language like commands. Labels maybe used to identify program segments and can be called from the main program providing sophisticated patterns for the debug of hardware or software.



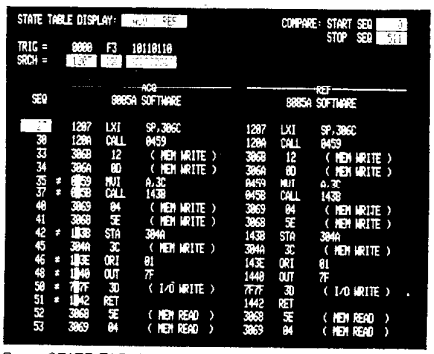
Press START SYSTEM: Data acquisition and pattern generator modules are simultaneously started. When a trigger occurs the DAS immediately defaults to the STATE TABLE format display with the trigger word clearly indicated on screen. Acquisition or pattern generator modules may be started separately by using the START ACQUISITION or START PAT GEN keys.



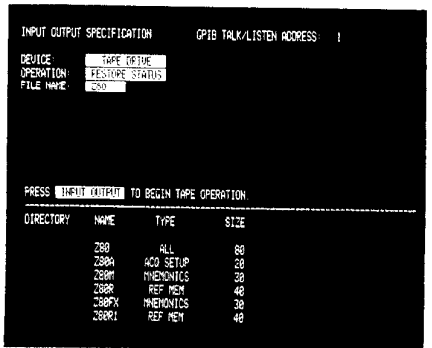
Press TIMING DIAGRAM: Instantly all acquired data is displayed with trigger word clearly indicated. Use SCROLL keys to make DELTA-TIME measurements or CURSOR keys to turn glitches on or off. Select magnification values from X1 to X10,000. Add labels for each channel using DATA ENTRY keys.



Press DEFINE MNEMONICS: Extended Define Mnemonics (EDM) provides complete disassembly capability to the DAS state table display. You can use it to disassemble any type of acquired data, whether from microprocessors, mini- or microcomputer, or buses. EDM is controlled by three submenus accessed via the DEFINE MNEMONICS menu key.



Press STATE TABLE: Reference memory is loaded by pressing STORE. REF MEM may be edited prior to doing an ACQ MEM and REF MEM compare. Display ACQ MEM ONLY, REF MEM ONLY or both by using SELECT key. A SEARCH word may be entered and the search started by pressing the SEARCH key.



Press INPUT OUTPUT: An I/O menu appears allowing the user to easily store or retrieve instrument setups, reference patterns and mnemonic (EDM) files and to define parameters for GPIB, RS-232, Master/Slave and serial Line Printer operation.

DAS 9100 CHARACTERISTICS

DATA FORMATTING

Group Designations — Up to 16 groups (1 to 32 channels per group).
Display Order — Designated group display order for state table.
Channel Order — Designated channel order within a group.
Radix — Octal, Binary, or Hexadecimal.
Polarity — Positive or negative (complement).
Threshold — Select TTL or variable.

TRIGGERING

Trigger — Synchronous or Asynchronous.
Trigger Word Position — Begin, Center, End of Memory.
Trigger Delay — 1 to 32,767 clock samples.
Trigger Word Display — Hex, Binary, Octal, or mixed radix; any bits allowed as don't care (X).
Trigger Modes (Word Recognition)
Up to five word recognizers with sixteen level stack (module dependent, see individual acquisition module specs)
- External Trigger Enable (TTL)
- Word Recognizer Output (TTL)
- 91A32 arms 91A08 or 91A04A/91AE04A
- 91A24 arms 91A08 or 91A04A/91AE04A
- 91A32 and 91A08
- Compare until equal or not equal

Glitch Recognizer (91A08 only)
- Enable by channel
- OR'ed with 91A08 trigger word

Clocks — See individual module specs.
Clock Qualifiers — See individual module specs.

DATA ACQUISITION DISPLAY MODES

Timing Diagram Features
- Simultaneous display of 16 user selectable channels
- User definable six-character trace labels for each displayed channel
- Data magnification factors from X1 to X10,000
- Cursor position and word readout in binary
- Search word
- Time aligned data display for arming mode
- Glitch display select (91A08 only)
- Horizontal data scrolling
- Memory display window
- Delta time measurement cursors

State Table Features
- Hex, Binary, Octal, or mixed radix
- Definable mnemonics displayed by group in acquisition/reference memory displays
- Search word
- Time-aligned data display for arms mode
- Vertical or block scrolling
- Cursor position
- Up to 1023 bits by 96 channels reference memory display, with or without data acquisition display
- Reference memory editing
- Programmable compare window
- Reference memory mask word capability
- Compare mode — highlighted and flagged for differences

Extended Define Mnemonics
- Software disassembly mode
- Hardware disassembly mode
- Absolute disassembly mode
- Simultaneous display of any two modes (Dependent on processor and mode selected)

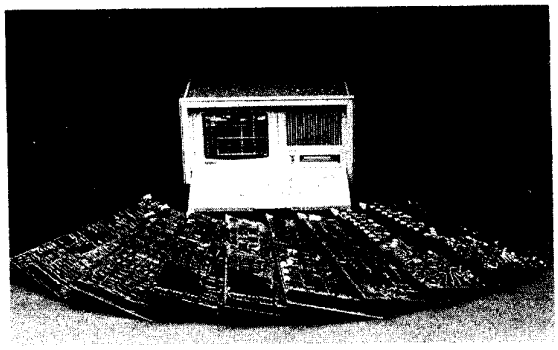
Up to 64 nestable tables with 256 entries per table. More than sufficient to completely disassemble 80186 and 68000 type processors.

KEYBOARD

The DAS 9100 keyboard is divided into four sections for ease of use and functionality. Menu keys, data entry keys, edit and cursor control, and system control keys provide total control at your fingertips.

I/O SUMMARY

DC 100 Tape Drive (Option 01)
Stores six full instrument setups or 20 different reference memory patterns. Directory space for 32 files.
RS-232 (Option 06)
Selectable Baud Rates: 300, 600, 1200, 2400, 4800, 9600.
Master/Slave Operation: Full Duplex, Asynchronous



GPIB (Option 06)
Talker/Listener Only.
Selectable Address.
Selectable Controller Type, EOI or (LF or EOI).
Line Printer Output (Option 06)
Prints both state and timing diagram.
RS-232 serial printers supported.
Selectable baud rates to 9600 baud.
Supports CTRL/S and CTRL/Q handshaking (X-on/X-off).
Composite Video Output (Option 06)
Hardcopy interface.
Video monitor interface.

OTHER CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Dimensions	mm	in
Width	432	17.0
Height	241	9.5
Depth	597	23.5
Weight	**kg**	**lb**
Without Accessories	21.8	48.0

LO Line — 90 V to 132 V RMS.
HI Line — 180 V to 264 V RMS.
Line Frequency — 48 Hz to 63 Hz.
Power — 1000 VA, maximum.
Temperature Range — Operating: 0°C to +50°C (+32°F to +122°F).
Storage: 40°C to +65°C (−40°F to +149°F).
Altitude — Operating: 10,000 ft maximum.
Storage: 50,000 ft. maximum.

INCLUDED PROBE ACCESSORIES

P6452 probe, 1 ea; P6454 external clock probe, 1 ea.

ORDERING INFORMATION

MAINFRAME ONLY

DAS 9109 Monochrome Mainframe ... **$5,500**
DAS 9119 ATE Mainframe (Deletes CRT and Keyboard; Adds Option 06) **$6,350**
DAS 9129 Color Mainframe **$8,400**

MAINFRAME OPTIONS

Option 01 — DC-100 Tape Drive ..... **+$1,450**
Option 03 — One Additional Power Supply ..... **+$800**
Option 04 — Two Additional Power Supplies ..... **+$1,600**
Option 05 — Rackmount Hardware ..... **+$200**
Option 06 — High-Speed GPIB, Serial Line Printer Port ..... **+$1,550**
Option 88 — Mainframe shipped with modules installed and checked out as part of the mainframe ..... **NC**

INTERNATIONAL POWER CORD AND PLUG OPTIONS

Option A1 — Universal Euro, 220 V/16 A, 50 Hz
Option A2 — UK, 240 V/13 A, 50 Hz
Option A3 — Australian, 240 V/10 A, 50 Hz
Option A4 — North American, 240 V/15 A, 60 Hz
Option A5 — Switzerland, 220 V/10 A, 50 Hz

MAINFRAME FIELD INSTALLABLE OPTIONS

DAS 91F1 — Field Installed Option 01 (Includes Installation in Service Center) **$1,700**
DAS 91F3 — Field Installed Additional Power Supply ... **$800**
DAS 91F6 — Field Installed Option 06 (For Mainframes Above S/N B020100) **$1,700**
Option 01 — Field Installed Option 06 (For Mainframes Below S/N B020100) ..... **NC**

MAINFRAME MODULES

The following modules include probes. See probe selection guide at end of this order section and pages (129 through 132) for additional module and probe selection information. Maximum of six modules per mainframe, 104 data acquisition channels and 80 pattern generator channels.

91AE04A — Data Acquisition Expansion Module **$5,950**
91AE24 — Data Acquisition Expansion Module **$4,700**
91A04A — Data Acquisition Module **$7,950**
91A08 — Data Acquisition Module **$3,985**
91A24 — Data Acquisition Module **$4,990**
91A32 — Data Acquisition Module **$4,990**
91P16 — Pattern Generator Module **$3,990**
91P32 — Pattern Generator Expansion Module **$6,900**

Note: When adding modules, check that the correct number of power supplies are also selected. The mainframe includes sufficient power for two modules. One additional power supply (Option 03) is required for three or four modules. Two additional power supplies (Option 04) are required for a total of five or six modules.
Microprocessor/Bus support: For ordering information please see page 123.

PROBES

P6452 — Eight Channel Data Acquisition Probe **$730**
P6453 — Four Channel High-Speed Data Acquisition Probe **$1,560**
P6454 — External Clock Probe For 91A08 Modules. (Only one required, included with each DAS 9100 Mainframe.) **$265**
P6455 — Eight Channel TTL/MOS Pattern Generator Probe **$575**
P6456 — Eight Channel ECL Pattern Generator Probe **$575**
P6457 — Four Channel Tri-State Pattern Generator Probe **$575**
P6460 — Eight Channel Data Acquisition Probe **$700**
P6462 — Eight Channel TTL Only Data Acquisition Probe **$340**

PROBE SELECTION GUIDE

DAS Module	No. Probes Required	Included As Standard	Optionally Available
91A04A	1	P6453	
91AE04A	1	P6453	
91A08	1	P6452	
91A24	3	P6460	P6462
91AE24	3	P6460	P6462
91A32	4	P6452	P6462
91P16	2	P6455	P6456, P6457
91P32	4	P6455	P6456, P6457

OPTIONAL ACCESSORIES

DAS Setup and Hold Calibration Fixture — Order 067-1037-00 ..... **$1,200**
High Speed Acquisition Test Fixture for 91A04A — Order 067-1139-00 ..... **$250**

For additional accessories please see pages 129 thru 132.

Select the Performance and Price That Meets Your Application Need.
The DAS 9100 is a modular architecture system designed to keep you state-of-the-art as your application needs change and grow. The modular DAS 9100 mainframe accepts up to six modules chosen from the selection of Data Acquisition and Pattern Generation modules listed on page 110 and 111.

The standard DAS 9100 mainframes with their associated options are shown on page 113. These DAS 9100 mainframes come standard with two module slots already powered. Options 03 and 04 allow you to add one or two power supplies, with each power supply providing power for two additional module slots. You only pay for the capability you need.

The Standard Configurations shown below provide an easy way to order a DAS already configured for your application. Use the chart below to match your application with the appropriate standard configuration.

Microprocessor Support.
The widest Selection of microprocessor support packages in the industry is listed on page 123.

DAS 9100 STANDARD CONFIGURATIONS ORDERING GUIDE

Standard Configuration Model Number		Recommended Application	Acquisition Modules	Pattern Generation Modules	Options Included	Performance Features
Color Display	Monochrome Display					
DAS 9121 $16,370	DAS 9101 $13,470	General Purpose Hardware Analysis	Two 91A08			16 Channel 100 MHz Data Acquisition
DAS 9122 $17,380	DAS 9102 $14,480	General Purpose Acquisition With Stimulus	One 91A32	One 91P16		32 Channel 25 MHz Data Acquisition 16 Channel 25 MHz Pattern Generation
DAS 9123 $22,165	DAS 9103 $19,265	General Purpose Software/Hardware Integration	One 91A32 One 91A08	One 91P16	Opt 03 Power	32 Channel 25 MHz Data Acquisition 8 Channel 100 MHz Data Acquisition 16 Channel 25 MHz Pattern Generation
DAS 9124 $33,390	DAS 9104 $30,490	Expanded Software/Hardware Integration	Two 91A32 Two 91A08	One 91P16	Opt 01 Tape Opt 04 Power	64 Channel 25 MHz Data Acquisition 16 Channel 25 MHz Pattern Generation 16 Channel 25 MHz Pattern Generation DC 100 Tape Mass Storage
DAS 9125 $19,540	DAS 9105 $16,640	General Purpose Microprocessor Support	One 91A24 One 91AE24		Opt 01 Tape	48 Channel 10 MHz Data Acquisition DC 100 Tape Mass Storage
DAS 9126 $24,550	DAS 9106 $21,650	High Speed Hardware Analysis	One 91A04A One 91AE04A		Opt 01 Tape Opt 03 Power	4 Channel 660 MHz or 8 Channel 330 MHz Data Acquisition DC 100 Tape Mass Storage
DAS 9127 $28,315	DAS 9107 $25,415	Microprocessor Software/Hardware Integration	One 91A24 One 91AE24 One 91A08	One 91P16	Opt 01 Tape Opt 03 Power	48 Channel 10 MHz Data Acquisition 8 Channel 100 MHz Data Acquisition 16 Channel 25 MHz Pattern Generation DC 100 Tape Mass Storage
DAS 9128 $45,760	DAS 9108 $42,860	Interactive ATE: VLSI Verification	Three 91A32	One 91P16 Two 91P32	Opt 01 Tape Opt 04 Power Opt 06 Comm	96 Channel 25 MHz Data Acquisition 80 Channel 25 MHz Pattern Generation DC 100 Tape Mass Storage GPIB/RS-232 Communications Interface Serial Line Printer Port Display Video Output
DAS 9118 $40,710 with DAS 9119 ATE mainframe		Remote Only Operation: Display and Keyboard Not Included	Three 91A32	One 91P16 Two 91P32	Opt 04 Power Opt 06 Comm	96 Channel 25 MHz Data Acquisiton 80Channel 25 MHz Pattern Generation CRT and Keyboard Deleted GPIB/RS-232 Communications Interface Serial Line Printer Port Display Video Output

DAS PERFORMANCE SUMMARY GUIDE

Module Name	Type	Channels	Maximum Channels	Memory Depth	Speed	Application
91A04A/91AE04A	Acquisition	2/4	16	4096/2048	660/330 MHz	High Speed Hardware Analysis
91A08	Acquisition	8	32	512	100 MHz	Hardware Analysis
91A32	Acquisition	32	96	512	25 MHz	Hardware/Software Analysis
91A24/91AE24	Acquisition	24	96	1023	10 MHz	Sophisticated Software Analysis
91P16/91P32	Pattern Generator	16/32	80	254	25 MHz	Hardware/Software Simulation